AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A Reed-Solomon decoder comprising:

a storing part;

a calculation part for calculating an error location and an error value from (2m) bit data from the storing part; and

a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part to output a decoded signal;

wherein m is an integer value, and the calculation part comprises:

a first RS core for calculating a first error location and a first error value from the data read from the storing part; and

a second RS core for calculating a second error location and a second error value from the data read from the storing part.

2. (original): The decoder according to claim 1, wherein the calculation part comprises:

an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag from the storing part;

a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part;

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a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part;

a first errata location polynomial calculation part for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial, and outputting the first errata location polynomial and the delayed first syndrome polynomial;

a first error location/value calculation part for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial;

a second errata location polynomial calculation part for calculating a second errata location polynomial from the calculated eraser location polynomial and second syndrome polynomial, and outputting the second errata location polynomial and the delayed second syndrome polynomial; and

a second error location/value calculation part for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial.

3. (canceled)

4. (previously presented): The decoder according to claim 1, wherein the first RS core comprises:

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an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part;

a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part;

a first errata location polynomial calculation part for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial, and outputting the first errata location polynomial and the delayed first syndrome polynomial; and

a first error location/value calculation part for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial.

5. (original): The decoder according to claim 4, wherein the first syndrome polynomial calculation part satisfies $S_j = \alpha^j(S_{j-1}\alpha^j+UM)+DM$ when (2m) bit data is inputted; and satisfies $S_j = S_{j-1}\alpha^j+UM$ when (m) bit data is inputted, wherein S; indicates a current state syndrome polynomial, S_{j-1} is a preceding state syndrome polynomial, α^j is a root of a generated polynomial, UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

6. (original): The decoder according to claim 4, wherein the first syndrome polynomial calculation part comprises:

a first syndrome storing part for temporarily storing a calculation result of the first syndrome polynomial;

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a first multiplier for multiplying the syndrome polynomial from the first syndrome storing part by a root α^j(j=0, 1, ..., N-K-1) of the generated polynomial;

a first adder for adding the output from the first multiplier to up (m) (UM) bits of the input data;

a first (m) bit multiplexer for outputting 1 or α^j according to the (m) or (2m) bit mode;

a second multiplier for multiplying the output from the first adder by the output from the first (m) bit multiplexer;

a second (m) bit multiplexer for outputting 0 or down (m) (DM) bits of the input data according to the (m) or (2m) bit mode; and

a second adder for adding the output from the second multiplier to the output from the second (m) bit multiplexer, the first syndrome storing part temporarily storing and outputting the output from the second adder;

wherein UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

7. (original): The decoder according to claim 4, wherein the second RS core comprises:

a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part;

a second errata location polynomial calculation part for calculating a second errata location polynomial from the calculated eraser location polynomial and second syndrome

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polynomial, and outputting the second errata location polynomial and the delayed second syndrome polynomial; and

a second error location/value calculation part for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial.

8. (original): The decoder according to claim 7, wherein the second syndrome polynomial calculation part satisfies $S_j = \alpha^j(S_{j-1}\alpha^j+UM)+DM$ when (2m) bit data is inputted; and satisfies $S_j = S_{j-1}\alpha^j+DM$ when (m) bit data is inputted, wherein S_j indicates a current state syndrome polynomial, S_{j-1} is a preceding state syndrome polynomial, α^j is a root of a generated polynomial, UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

9. (original): The decoder according to claim 7, wherein the second syndrome polynomial calculation part comprises:

a second syndrome storing part for temporarily storing a calculation result of the second syndrome polynomial;

a third (m) bit multiplexer for outputting 1 or α^j according to the (m) or (2m) bit mode;

a third multiplier for multiplying the output from the second syndrome storing part by the output from the third (m) bit multiplexer;

a fourth (m) bit multiplexer for outputting 0 or up (m) (UM) bits of the input data according to the (m) or (2m) bit mode;

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a third adder for adding the output from the third multiplier to the output from the fourth (m) bit multiplexer; and

a fourth multiplier for multiplying the output from the third adder by a root α^j(j=0, 1, ..., N-K-1) of the generated polynomial; and

a fourth adder for adding the output from the fourth multiplier to down (m) (DM) bits of the input data, the second syndrome storing part storing and outputting the output from the fourth adder;

wherein UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

10. (previously presented): A Reed-Solomon decoder for processing (m) or (2m) bit data, comprising:

a storing part for storing (2m) bit data;

a main control part for controlling the storing part;

a first RS core for calculating a first error location and a first error value from the data read from the storing part;

a first RS core control part for controlling the first RS core under the control of the main control part;

a second RS core for calculating a second error location and a second error value from the data read from the storing part; and

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a second RS core control part for controlling the second RS core under the control of the main control part;

wherein m is an integer value.

11. (original): The decoder according to claim 10, wherein the first RS core comprises:

an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag from the storing part;

a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part;

a first errata location polynomial calculation part for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial, and outputting the first errata location polynomial and the delayed first syndrome polynomial; and

a first error location/value calculation part for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial.

12. (original): The decoder according to claim 11, wherein the first syndrome polynomial calculation part comprises:

a first syndrome storing part for temporarily storing a calculation result of the first syndrome polynomial;

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a first multiplier for multiplying the syndrome polynomial from the first syndrome storing part by a root α^j(j=0, 1, ..., N-K-1) of the generated polynomial;

a first adder for adding the output from the first multiplier to up (m) (UM) bits of the input data;

a first (m) bit multiplexer for outputting 1 or α^j according to the (m) or (2m) bit mode;

a second multiplier for multiplying the output from the first adder by the output from the first (m) bit multiplexer;

a second (m) bit multiplexer for outputting 0 or down (m) (DM) bits of the input data according to the (m) or (2m) bit mode; and

a second adder for adding the output from the second multiplier to the output from the second (m) bit multiplexer, the first syndrome storing part temporarily storing and outputting the output from the second adder;

wherein UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

13. (previously presented): The decoder according to claim 10, wherein the second RS core comprises:

a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part;

a second errata location polynomial calculation part for calculating a second errata location polynomial from a calculated eraser location polynomial and second syndrome

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polynomial, and outputting the second errata location polynomial and the delayed second syndrome polynomial; and

a second error location/value calculation part for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial.

14. (original): The decoder according to claim 13, wherein the second syndrome polynomial calculation part comprises:

a second syndrome storing part for temporarily storing a calculation result of the second syndrome polynomial;

a third (m) bit multiplexer for outputting 1 or α^j according to the (m) or (2m) bit mode;

a third multiplier for multiplying the output from the second syndrome storing part by the output from the third (m) bit multiplexer;

a fourth (m) bit multiplexer for outputting 0 or up (m) bits of the input data according to the (m) or (2m) bit mode;

a third adder for adding the output from the third multiplier to the output from the fourth (m) bit multiplexer; and

a fourth multiplier for multiplying the output from the third adder by a root α^j(j=0, 1, ..., N-K-1) of the generated polynomial; and

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a fourth adder for adding the output from the fourth multiplier to down (m) bits of the input data, the second syndrome storing part storing and outputting the output from the fourth adder.

15. (previously presented): A Reed-Solomon decoding method comprising the steps of:

reading data to be decoded and an eraser flag;

calculating an error location and an error value from the read data; and

correcting an error of the data according to the calculated error location and error value, and decoding the data;

wherein the calculation step comprises:

a first calculation step for calculating a first error location and a first error value from the read data; and

a second calculation step for calculating a second error location and a second error value from the read data.

16. (original): The method according to claim 15, wherein the data is read in (2m) bit units in the data reading step.

17. (previously presented): A Reed-Solomon decoding method comprising the steps of:

reading data to be decoded and an eraser flag;

calculating an error location and an error value from the read data; and

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correcting an error of the data according to the calculated error location and error value, and decoding the data;

wherein the data reading step comprises:

an eraser location polynomial calculation step for calculating an eraser location polynomial from the read eraser flag;

a first syndrome polynomial calculation step for calculating a first syndrome polynomial from the read data;

a second syndrome polynomial calculation step for calculating a second syndrome polynomial from the read data;

a first errata location polynomial calculation step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial, and outputting the first errata location polynomial and the delayed first syndrome polynomial;

a first error location/value calculation step for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial;

a second errata location polynomial calculation step for calculating a second errata location polynomial from the calculated eraser location polynomial and second syndrome polynomial, and outputting the second errata location polynomial and the delayed second syndrome polynomial; and

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a second error location/value calculation step for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial.

18. (canceled)

19. (previously presented): The method according to claim 15, wherein the first calculation step comprises:

an eraser location polynomial calculation step for calculating an eraser location polynomial from the read eraser flag;

a first syndrome polynomial calculation step for calculating a first syndrome polynomial from the read data;

a first errata location polynomial calculation step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial, and outputting the first errata location polynomial and the delayed first syndrome polynomial; and

a first error location/value calculation step for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial.

20. (original): The method according to claim 19, wherein the first syndrome polynomial calculation step satisfies $S_j = \alpha^j(S_{j-1}\alpha^j+UM)+DM$ when (2m) bit data is inputted; and satisfies S_j

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$= S_{j-1}\alpha^{j}+UM$ when (m) bit data is inputted, wherein S_j; indicates a current state syndrome polynomial, S_{j-1} is a preceding state syndrome polynomial, α^{j} is a root of a generated polynomial, UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

21. (previously presented): The method according to claim 15, wherein the second calculation step comprises:

a second syndrome polynomial calculation step for calculating a second syndrome polynomial from the read data;

a second errata location polynomial calculation step for calculating a second errata location polynomial from a calculated eraser location polynomial and second syndrome polynomial, and outputting the second errata location polynomial and the delayed second syndrome polynomial; and

a second error location/value calculation step for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial.

22. (original): The method according to claim 21, wherein the second syndrome polynomial calculation step satisfies $S_j = \alpha^{j}(S_{j-1}\alpha^{j}+UM)+DM$ when (2m) bit data is inputted; and satisfies $S_j = S_{j-1}\alpha^{j}+DM$ when m bit data is inputted, wherein S_j indicates a current state syndrome polynomial, S_{j-1} is a preceding state syndrome polynomial, α^{j} is a root of a generated polynomial, UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

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23-27. (canceled).

28. (original): The decoder according to claim 12, wherein the first syndrome polynomial calculation part satisfies $S_j = \alpha^j(S_{j-1}\alpha^j+UM)+DM$ when (2m) bit data is inputted; and satisfies $S_j = S_{j-1}\alpha^j+UM$ when (m) bit data is inputted, wherein Sj indicates a current state syndrome polynomial, S_{j-1} is a preceding state syndrome polynomial, α^j is a root of a generated polynomial, UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

29. (original): The decoder according to claim 14, wherein the second syndrome polynomial calculation part satisfies $S_j = \alpha^j(S_{j-1}\alpha^j+UM)+DM$ when (2m) bit data is inputted; and satisfies $S_j = S_{j-1}\alpha^j+DM$ when (m) bit data is inputted, wherein S_j indicates a current state syndrome polynomial, S_{j-1} is a preceding state syndrome polynomial, α^j is a root of a generated polynomial, UM is up (m) bits of the (2m) bit data, and DM is down (m) bits of the (2m) bit data.

30. (original): The method according to claim 15, wherein the correcting an error step comprises:

a first error correction step for correcting the read data from the first error value and the first error location from the read data; and

a second error correction step for correcting the read data from the second error value and the second error location from the read data.

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31. (previously presented): The decoder according to claim 1, wherein m is a number of bits which may be appropriately determined according to a data representation method, and which represents an amount of data able to be processed by one of the cores of the decoder.

32. (previously presented): The decoder according to claim 1, wherein the first RS core and the second RS core operate in parallel.

33. (previously presented): The decoder according to claim 10, wherein m is a number of bits which may be appropriately determined according to a data representation method, and which represents an amount of data able to be processed by one of the cores of the decoder.

34. (previously presented): The decoder according to claim 10, wherein the first RS core and the second RS core operate in parallel.

35. (previously presented): The method according to claim 15, wherein the first calculation step and the second calculation step are concurrently performed.

36. (previously presented): The method according to claim 16, wherein m is a number of bits which may be appropriately determined according to a data representation method, and which represents an amount of data able to be processed by one of the first and second calculation steps.

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